REMARKS

Claims 1-4, 11-14, 17-22 and 43-53 were pending in the application. By this paper, Claims 14, 43-49 and 52-53 have been cancelled without prejudice, Claims 1, 3, 11, 12, 17, 19 and 50 have been amended, and new Claims 54-61 added. Hence, Claims 1-4, 11-13, 17-22, 50-51 and 54-61 are now pending in the application.

Request for Continued Examination (RCE)

Applicant files herewith an RCE for continued prosecution of the above-referenced application.

Withdrawn Claims

Per page 2 of the Office Action, claims 43-49 and 52-53 were withdrawn from consideration as being directed to a non-elected invention per 37 CFR 1.142(b) and MPEP § 821.03. Applicant has herein cancelled claims 43-49 and 52-53 without prejudice.

Claim Rejections Under 35 U.S.C. §102

Claim 3 – Per page 3 of the Office Action, Claim 3 stands rejected as being anticipated by Shapiro et al. (US 4,899,128, hereinafter "Shapiro"). Applicant has herein amended Claim 3 such that the recited plurality of strings of data are generated by a plurality of processors within said at least one data processing device operating on a same task. Support for this amendment can be found, *inter alia*, at page 18, line 29 through page 19, line 6 of Applicant's specification. Applicant submits that Shapiro can not, as a matter of law, anticipate Claim 3 as amended; specifically Applicant believes that Shapiro does not explicitly disclose a processor, yet alone a plurality of processors within said at least one data processing device.

Further, Applicant submits that Claim 3 as amended is both novel and non-obvious over the prior art, including those other references specifically cited by the Examiner in this Office Action. For example, while Baird, et al. (US 5,848,264, hereinafter "Baird") teaches a microprocessor die containing multiple processor cores and a method for debugging the same, Applicant believes that Baird actually teaches away from Applicant's claimed invention.

Specifically, Baird seemingly never contemplates analyzing a plurality of strings of data generated by a plurality of processors operating on a *same task*. Rather, Baird seemingly only contemplates "processor cores [that] are capable of simultaneously executing *independent* programs." (See e.g., Col. 2, lines 30-32; Col. 4, lines 26-27; Col. 10, lines 3-4; Claims 10, 17). As Baird only contemplates a method of handling the bandwidth of a plurality of events occurring on processor cores executing independent programs, Applicant submits that Baird teaches away form the concept of analyzing a plurality of strings of data generated by a plurality of processors operating on a *same* task. Applicant submits that Claim 3 as amended, and Claim 4 which depends directly therefrom, are therefore in condition for allowance.

Claim 19 – Per pages 3-4 of the Office Action, Claim 19 stands rejected as being anticipated by Baird. Applicant has herein amended Claim 19 to further include the limitation "wherein said first and second software processes are *a same task*". Support for this amendment can be found, *inter alia*, at page 18, line 29 through page 19, line 6 of Applicant's specification. Applicant's reading of Baird suggests that Baird never contemplated a first and second software process, where these two processes comprise a same task; rather Baird seemingly only contemplates the execution of *independent* programs (See e.g., Col. 2, lines 30-32; Col. 4, lines 26-27; Col. 10, lines 3-4; Claims 10, 17). Applicant submits that Baird is primarily concerned with methods of handling the increased bandwidth necessary to debug a multi-processor core running independent programs.

Applicant therefore respectfully submits that Claim 19 as amended, and Claim 22 which depends therefrom, distinguish over the prior art and thus are in condition for allowance.

Claim Rejections Under 35 U.S.C. §103

Claim 1 – Per pages 5-6 of the Office Action, Claim 1 stands rejected as being unpatentable under Section 103 over Kernighan et al., "*The Practice of Programming*", (hereinafter "Kernighan") in view of Baird. Applicant has herein amended Claim 1 to include limitations relating to a plurality of input strings of data being generated by a same task. Support for this amendment can be found, *inter alia*, at page 18, line 29 through page 19, line 6 of

Applicant's specification. As previously discussed, Baird seemingly never contemplated analyzing a plurality of strings of data generated by a *same task*. Rather, Baird seemingly only contemplates "processor cores [that] are capable of simultaneously executing *independent* programs." (See e.g., Col. 2, lines 30-32; Col. 4, lines 26-27; Col. 10, lines 3-4; Claims 10, 17). Applicant therefore submits that not only does Baird and Kernighan not teach each and every limitation of Claim 1, Baird actually teaches away from Claim 1 as amended herein, as Baird seemingly only contemplated *independent* programs.

Further, Applicant has also amended Claim 1 to include the limitation of "analyzing said groups of said data for potential hardware or software integration problems associated with one or more of said data processors based at least in part on said differences between said plurality of strings." Support for this amendment can be found, *inter alia*, at page 19, lines 1-6 of Applicant's specification. Applicant believes that Baird does not teach nor suggest such functionality. Applicant therefore respectfully submits that Claim 1 and all claims depending either directly or indirectly therefrom are in condition for allowance.

Claims 11 and 12 – Per pages 12-13 of the Office Action, Claims 11 and 12 stand rejected under Section 103 as being unpatentable over Shapiro in view of Aho et al., "*Compilers, Principles, Techniques, and Tools*" (hereinafter "Aho"). Both Claims 11 and 12 have herein been amended to include limitations wherein said at least one data processing device has a plurality of processor cores, said cores each operating on a same task. Support for this amendment can be found, *inter alia*, at page 18, line 29 through page 19, line 6 of Applicant's specification. Applicant submits that neither Aho nor Shapiro contemplate a data processing device having a plurality of processor cores.

Further, Applicant has also amended Claims 11 and 12 to include limitations relating to analyzing said groups of said data for potential hardware or software integration problems associated with one or more of said plurality of processor cores based at least in part on said relationship between said plurality of strings. Support for Applicant's amendment can be found, *inter alia*, pages 18-19 of Applicant's specification. Applicant submits that none of the prior art, including those references specifically cited by the examiner in this Office Action (i.e., Aho,

Shapiro, Baird and Kernighan) teach or suggest, *inter alia*, "analyzing said groups of said data for potential hardware or software integration problems associated with one or more of said plurality of processor cores *based at least in part on said relationship* between said plurality of strings (generated by the *same task*)". Applicant respectfully submits that Claims 11 and 12 and all claims depending directly or indirectly therefrom are in condition for allowance

Claim 17 – Per pages 7-8 of the Office Action, Claim 17 stands rejected as being unpatentable over Kernighan in view of Baird. Applicant has herein amended Claim 17 to further distinguish over the cited prior art. Specifically, Applicant has amended Claim 17 to include generating a first, second and third data string from a first, second and third digital processor respectively using a first software process. Support for this amendment can be found, *inter alia,* at page 18, lines 18-25 of Applicant's specification. Applicant submits that Claim 17 is distinguishable over the disclosure in Baird as Baird is concerned generally with being able to debug multiple independent software processes running on different cores within the *same die* (see e.g., Baird's Abstract). The main alleged advantage from Applicant's reading of Baird is that Baird enables concurrent debugging without burdening the bandwidth of the memory bus of the microprocessor. See, e.g., *Col. 10, lines 55-67.* Claim 17 as presented herein, on the other hand, deals with a debug process on a *plurality of digital processors*. Applicant believes the usefulness of the Baird approach would be lost as applied to a plurality of digital processors, as bandwidth concerns would be moot under Applicant's approach.

Applicant therefore submits that even if each element of amended Claim 17 were taught in Baird and Kernighan, which Applicant submits is not the case, there would be no objective motivation or suggestion to combine the teachings of Baird with that of Kernighan to create the invention of Claim 17 as the problem Baird attempts to solve would not be present in Claim 17 as amended.

Further, although the Examiner cites the objective motivation to combine Kernighan and Baird because of an "increase in debug/test capacity for quicker more efficient execution", Applicant submits that the teaching of Baird as it is applied to the invention of amended Claim

17 would not work for its intended purpose, i.e., there would be no need to use the invention of Baird as bandwidth would not be an issue for an invention such as that set forth in Claim 17.

Applicant therefore submits that Claim 17, and Claim 18 which depends directly therefrom, distinguish over the prior art, including those references cited by the Examiner, and are in condition for allowance.

Claim 50 – Per page 14 of the Office Action, Claim 50 stands rejected as being unpatentable over Shapiro in view of Aho. Applicant has herein amended Claim 50 to include the added step of "generating said plurality of inputs of data by running a same task on respective ones of said plurality of data processors." Claim 50 also includes the added step of "analyzing said at least one relationship among said plurality of inputs of data, said act of analyzing finding areas of the design which may require refinement or verification." Support for these amendments can be found, *inter alia*, at pages 18-19 of Applicant's specification. Neither Aho nor Shapiro teach or suggest such functionality as set forth in amended Claim 50.

Further, although the Examiner has not specifically cited Baird with respect to Claim 50, Applicant believes that Baird teaches away from Claim 50 as amended. Specifically, Applicant's reading of Baird suggests that Baird only contemplates solving the problem where a debugging apparatus and the number of debug events that can occur, exceeds the bandwidth of the pins of the chip. Applicant believes there would be no objective motivation or suggestion to combine Baird with any reference as the problem Baird attempts to solve (i.e., debugging in an environment having limited bandwidth – e.g., a multi-processor core environment) would not be present in Applicant's amended Claim 50 invention.

In addition, Baird seemingly never contemplates generating said plurality of inputs of data by running a *same task*. Rather, Baird seemingly only contemplates "processor cores [that] are capable of simultaneously executing *independent* programs." (See e.g., Col. 2, lines 30-32; Col. 4, lines 26-27; Col. 10, lines 3-4; Claims 10, 17).

Applicant therefore respectfully submits that Claim 50, and Claim 51 depending directly therefrom, are in condition for allowance.

New Claims

Applicant has herein added new claims 54-61. Support for these new claims is replete throughout the specification, and hence no new matter has been added. Specifically, support can be found as follows:

Claim 54 – Support for this claim can generally be found, *inter alia*, at page 18, lines 26-28 of Applicant's specification.

Claims 55-57 – Support for these dependent claims can generally be found, *inter alia*, at page 21, lines 4-5 of Applicant's specification.

Claim 58 – Support for this claim can generally be found, *inter alia*, at page 18, lines 26-28 and page 19, lines 7-13 of Applicant's specification.

Claim 60 – Support for this claim can generally be found, *inter alia*, at page 20, lines 1-8 of Applicant's specification.

Claim 61 – Support for this claim can generally be found, *inter alia*, at page 18, lines 18-28 of Applicant's specification.

Other Remarks

Based on the foregoing, Applicant respectfully submits that Claims 1-4, 11-14, 17-22, 50-51 and 54-61 define patentable subject matter, and are in condition for allowance.

Applicant hereby specifically reserves the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such cancellations or additions.

Furthermore, any remarks made with respect to a give claim or claims are limited to only such claim or claims.

If the Examiner has any questions or comments which may be resolved over the telephone, he is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

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